In the claims:

1. (Cancelled)

2. (Currently Amended) A delay adjustment circuit according to claim 7~~claim 1~~, wherein said control device is ~~being~~ provided on board the semiconductor integrated circuit device, ~~being~~ is formed to include a register that can set an output value that depends on an internal signal, and adjust a ~~adjusting the~~ gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the output~~register~~ value set in said register.

3. (Currently Amended) A delay adjustment circuit according to claim 7~~claim 1~~, wherein said control device is ~~being~~ provided on board the semiconductor integrated circuit device, is ~~being~~ formed to include a register that can set an ~~the~~ output value externally by initialization, and ~~adjusting~~ adjust a ~~the~~ gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the output ~~register~~ value set in said register.

4. – 6. (Cancelled)

7. (Currently Amended) A clock generating circuit comprising:

(1) the delay adjustment circuit

a) a first gate array that has each gate serially connected for carrying out fine adjustment of a delay time interval of an input signal;

b) a capacitance connected to an output side of a specified gate in the first gate array via a first switching device;

c) a second gate array that is connected to an output side of said first gate array via a second switching device and carries out rough adjustment of the delay time interval of said input signal; and

d) a control device that controls said first switching device and said second switching device so as to adjust the delay time interval of said input signal by adjusting the capacitance connected to the output side of the specified gate in the first gate array and the number of gate stages in the second gate array~~according to claim 1~~;

(2) a duty ratio detecting device that detects a ~~the~~ duty ratio of the clock output of this clock generating circuit; and

(3) a control device that automatically updates the output value set in said register ~~register value~~ in said delay adjustment circuit so as to become a pre-set duty ratio based on a~~the~~ detected output of said duty ratio detecting device.

8. (Currently Amended) A clock generating circuit comprising:

(1) the delay adjustment circuit which comprises:

a) a first gate array that has each gate serially connected for carrying out fine adjustment of a delay time interval of an input signal;

b) a capacitance connected to an output side of a specified gate in the first gate array via a first switching device;

c) a second gate array that is connected to an output side of said first gate array via a second switching device and carries out rough adjustment of the delay time interval of said input signal; and

d) a control device that controls said first switching device and said second switching device so as to adjust the delay time interval of said input signal by adjusting the capacitance connected to the output side of the specified gate in the first gate array and the number of gate stages in the second gate array;

e) wherein said control device is provided on board the semiconductor integrated circuit device, is formed to include a register that can set an output value that

depends on an internal signal, and adjust a gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the output value set in said register;

~~according to Claim 2;~~

(2) a clock skew detecting device that detects clock skew; and

(3) a control device that automatically updates the output value set in said register ~~register values~~ in said delay adjustment circuit so that the clock skew becomes a pre-set expected value based on a ~~the~~ detected output of said clock skew detecting device.

9. – 15 (Cancelled)

16. (New) A delay adjustment circuit according to claim 8, wherein said control device is provided on board the semiconductor integrated circuit device, is formed to include a register that can set an output value that depends on an internal signal, and adjust a gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the output value set in said register.

17. (New) A delay adjustment circuit according to claim 8, wherein said control device is provided on board the semiconductor integrated circuit device, is formed to include a register that can set an output value externally by initialization, and adjust a gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the output value set in said register.